Introduction To Semiconductor Manufacturing Technology

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CMOS Process Flow

• Overview of Areas in a Wafer Fab
  – Diffusion (oxidation, deposition and doping)
  – Photolithography
  – Etch
  – Ion Implant
  – Thin Films
  – Polish

• CMOS Manufacturing Steps
• Parametric Testing
• 6~8 weeks involve 350-step
Model of Typical Wafer Flow in a Sub-Micron CMOS IC Fab

6 major production areas
Clean: Types of Contamination and The Problems They Cause

• Particles
• Metallic Impurities
• Organic Contamination
• Native Oxides
• Electrostatic Discharge

• Contamination often leads to a defective chip. Killer defects are those causes of failure where the chip on the wafer fails during electrical test.
• It is estimated that 80% of all chip failure are due to killer defects from contamination.
## Wafer Wet-Cleaning Chemicals

<table>
<thead>
<tr>
<th>Contaminant</th>
<th>Name</th>
<th>Chemical Mixture Description (all Cleans are followed by a DI Water Rinse)</th>
<th>Chemicals</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Particles</strong></td>
<td><strong>SC-1</strong> (APM)</td>
<td>• Ammonium hydroxide/hydrogen peroxide/DI water</td>
<td>NH₄OH/H₂O₂/H₂O</td>
</tr>
<tr>
<td><strong>SC-1</strong> (APM)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Organics</strong></td>
<td><strong>SC-1</strong> (APM)</td>
<td>• Ammonium hydroxide/hydrogen peroxide/DI water</td>
<td>NH₄OH/H₂O₂/H₂O</td>
</tr>
<tr>
<td><strong>SC-1</strong> (APM)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Metallics (not Cu)</strong></td>
<td><strong>SC-2</strong> (HPM)</td>
<td>• Hydrochloric acid/hydrogen peroxide/DI water</td>
<td>HCl/H₂O₂/H₂O</td>
</tr>
<tr>
<td><strong>SC-2</strong> (HPM)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>SC-2</strong> (HPM)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Piranha (SPM)</strong></td>
<td></td>
<td>• Sulfuric acid/hydrogen peroxide/DI water</td>
<td>H₂SO₄/H₂O₂/H₂O</td>
</tr>
<tr>
<td><strong>Piranha (SPM)</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>DHF</strong></td>
<td></td>
<td>• Hydrofluoric acid/water solution (will not remove copper)</td>
<td>HF/H₂O</td>
</tr>
<tr>
<td><strong>Native Oxides</strong></td>
<td><strong>DHF</strong></td>
<td>• Hydrofluoric acid/water solution (will not remove copper)</td>
<td>HF/H₂O</td>
</tr>
<tr>
<td><strong>DHF</strong></td>
<td></td>
<td></td>
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</tr>
<tr>
<td><strong>DHF</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>BHF</strong></td>
<td></td>
<td>• Buffered hydrofluoric acid</td>
<td>NH₄F/HF/H₂O</td>
</tr>
<tr>
<td><strong>BHF</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>BHF</strong></td>
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</tr>
</tbody>
</table>
## Typical Wafer Wet-Cleaning Sequence

<table>
<thead>
<tr>
<th>Cleaning Step</th>
<th>What it Cleans</th>
</tr>
</thead>
<tbody>
<tr>
<td>H₂SO₄/H₂O₂ (piranha)</td>
<td>Organics &amp; metals</td>
</tr>
<tr>
<td>UPW rinse (ultrapure water)</td>
<td>Rinse</td>
</tr>
<tr>
<td>HF/H₂O (dilute HF)</td>
<td>Native oxides</td>
</tr>
<tr>
<td>UPW rinse</td>
<td>Rinse</td>
</tr>
<tr>
<td>NH₄OH/H₂O₂/H₂O (SC-1)</td>
<td>Particles</td>
</tr>
<tr>
<td>UPW rinse</td>
<td>Rinse</td>
</tr>
<tr>
<td>HF/H₂O</td>
<td>Native oxides</td>
</tr>
<tr>
<td>UPW rinse</td>
<td>Rinse</td>
</tr>
<tr>
<td>HCl/H₂O₂/H₂O (SC-2)</td>
<td>Metals</td>
</tr>
<tr>
<td>UPW rinse</td>
<td>Rinse</td>
</tr>
<tr>
<td>HF/H₂O</td>
<td>Native oxides</td>
</tr>
<tr>
<td>UPW rinse</td>
<td>Rinse</td>
</tr>
<tr>
<td>Drying</td>
<td>Dry</td>
</tr>
</tbody>
</table>

UPW: Ultrapure Water
Diffusion: Simplified Schematic of High-Temperature Furnace

- Temperature controller
- Thermocouple measurements
- Gas flow controller
- Process gas
- Quartz tube
- Heater 1
- Heater 2
- Heater 3
- Three-zone Heating Elements
- Pressure controller
- Exhaust

Can do: oxidation, diffusion, deposition, anneals, and alloy
Dry Oxidation Time (Minutes)

$Si\ (solid) + O_2\ (gas) \rightarrow SiO_2\ (solid)$

Oxide thickness (μm) vs Time (minutes)

- (100) Silicon
- Lines indicate temperatures:
  - 1200°C
  - 1100°C
  - 1000°C
  - 900°C
  - 800°C
  - 700°C
Wet Oxygen Oxidation

- $\text{H}_2 + \text{O}_2 \rightarrow \text{H}_2\text{O}$
- $\text{Si (solid)} + 2\text{H}_2\text{O} \rightarrow \text{SiO}_2 (\text{solid}) + 2\text{H}_2$
- The fast growth rate in wet atmosphere is due to the faster diffusion and higher solubility of water vapor than oxygen in silicon dioxide
- Hydrogen molecules produced in the reaction are trapped in oxide, less dense, using heating (annealing) to improve.
Negative Lithography

- Areas exposed to light become crosslinked and resist the developer chemical.
Positive Lithography

Areas exposed to light are dissolved.

Resulting pattern after the resist is developed.
Eight Steps of Photolithography

1) Vapor prime
2) Spin coat
3) Soft bake
4) Alignment and Exposure
5) Post-exposure bake
6) Develop
7) Hard bake
8) Develop inspect
Photolithography Bay in a Sub-micron Wafer Fab

- It is to photograph the image of a circuit pattern onto the photoresist that coats the wafer surface.
- Yellow fluorescent does not affect photoresist, but sensitive to UV
Simplified Schematic of a Photolithography Processing Module

Note: wafers flow from photolithography into only two other areas: *etch* and *ion implant*
Etch: Dissociation

• Electron collides with a molecule, it can break the chemical bond and generate free radicals:

\[ e + AB \rightarrow A + B + e \]

• **Free radicals** have at least one unpaired electron and are chemically very reactive.

• Increasing chemical reaction rate

• Very important for both etch and CVD.
Simplified Schematic of Dry Plasma Etcher

- The etch process creates a permanent pattern on the wafer in areas not protected by the photoresist pattern
- Including: dry etching, wet etching and photoresist stripper
- After dry etching: photoresist stripper + wet cleaning

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[Diagram of dry plasma etcher showing various components such as gas distribution baffle, Anode electrode, Electromagnetic field, Free electron, Ion sheath, Chamber wall, Positive ion, Radial chemical, Vacuum line, Exhaust to vacuum pump, High-frequency energy, RF coax cable, Photon, Glow discharge (plasma), Vacuum gauge, Wafer, Cathode electrode, Flow of byproducts and process gases, Etchant gas entering gas inlet.]
Wet Chemical Isotropic Etch

• Etch profile refers to the shape of the sidewall of the etched feature
• **Isotropic** etch profile leads to a undercutting, results in an undesirable **loss** of the linewidth

*Isotropic etch - etches in all directions at the same rate*
Anisotropic Etch with Vertical Etch Profile

- The rate of etching is on only one direction perpendicular to the wafer surface
- There is very little lateral etching activity
- This leaves vertical sidewalls, permitting a higher packing density of etched features on the chip
- With smaller geometries, the etch profiles have higher aspect ratios
- It is difficult to get etchant chemicals in and reaction by-products out of the high-aspect ratio openings

Anisotropic etch - etches in only one direction
Implantation: Common Dopants Used in Semiconductor Manufacturing

- **Doping** is the *introduction* of a dopant into the crystal structure of a semiconductor material to modify its electronic properties.
- Dopants are referred to as *impurities*.
- Two techniques: thermal diffusion and ion implantation (dominant)

<table>
<thead>
<tr>
<th>Acceptor Dopant Group IIIA (P-Type)</th>
<th>Semiconductor Group IVA</th>
<th>Donor Dopant Group VA (N-Type)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Element</td>
<td>Atomic Number</td>
<td>Element</td>
</tr>
<tr>
<td>Boron (B)</td>
<td>5</td>
<td>Carbon</td>
</tr>
<tr>
<td>Aluminum</td>
<td>13</td>
<td>Silicon (Si)</td>
</tr>
<tr>
<td>Gallium</td>
<td>31</td>
<td>Germanium</td>
</tr>
<tr>
<td>Indium</td>
<td>49</td>
<td>Tin</td>
</tr>
</tbody>
</table>
General Schematic of an Ion Implanter

- **Ion source**: positive charge
- **Extraction assembly**: extract ions
- **Mass Analyzer**: form a beam of the desired dopant ions
- **Acceleration column**: to attain a high velocity
Annealing of Silicon Crystal

Using Furnace or RTA, hot-wall furnace using high temperature causes extensive dopant diffusion and is undesirable.

RTA minimizes a phenomenon known as transient enhanced diffusion, to achieve acceptable junction depth control in shallow implants (~150°C/sec).
Thin Film Metallization Bay
Simple Parallel Plate DC Diode Sputtering System

1) Electric fields create Ar\(^+\) ions.
2) High-energy Ar\(^+\) ions collide with metal target.
3) Metallic atoms are dislodged from target.
4) Metal atoms migrate toward substrate.
5) Metal deposits on substrate.
6) Excess matter is removed from chamber by a vacuum pump.
Simplified Schematics of CVD Processing System

- Capacitive-coupled RF input
- Gas inlet
- Chemical vapor deposition
- Wafer
- Susceptor
- Heat lamps
- Exhaust
- CVD cluster tool
- Process chamber
Schematic of CVD Transport and Reaction 8 Steps

1) Mass transport of reactants

2) Film precursor reactions

3) Diffusion of gas molecules

4) Adsorption of precursors

5) Precursor diffusion into substrate

6) Surface reactions

7) Desorption of byproducts

8) By-product removal

Gas delivery

CVD Reactor

Exhaust

Substrate

Continuous film
CVD Reaction

- Take place on wafer surface: **heterogeneous** reaction (surface catalyzed).
- **Homogeneous** reaction: above surface (gas reaction), which is poor adhesion, low-density with high defects
- \( \text{SiH}_4 \rightarrow \text{SiH}_2 + \text{H}_2 \) (\( \text{SiH}_2 \) is **precursor**, it is pyrolysis)
- CVD reaction steps are **sequential**, the slowest step defines the bottleneck
LPCVD Reaction Chamber for Deposition of Oxides, Nitrides, or Polysilicon

Three-zone heating element

- Limited by surface reaction, flow condition is not important
- Films are uniformly deposited on a large number of wafer surface as long as the temperature is tightly controlled
- Conformal film coverage on the wafer
- Low growth rate than APCVD and need routine maintenance
- In-situ clean, using ClF$_3$ or NF$_3$
- $3\text{SiCl}_2\text{H}_2 + 4\text{NH}_3 \rightarrow \text{Si}_3\text{N}_4 + 6\text{HCl} + 6\text{H}_2$
Polish Bay in a Sub-micron Wafer Fab

- Chemical mechanical planarization (CMP) process is to **planarize** the top surface of the wafer by lowering the high topography to be level with the lower surface area of the wafer.
- It combines **chemical etching** and **mechanical abrading** to remove layer.
### Schematic of Chemical Mechanical Planarization (CMP)

**Step height:** etchback $\sim 7000\text{Å}$ vs. CMP $\sim 50\text{Å}$

- CMP achieves wafer planarity by removing high features on the surface more quickly relative to the low feature (high pressure by Preston’s eq.)
- Both metal and dielectric layers can be removed
Biasing Circuit for an NMOS Transistor

Figure 3.16

\[ V_{GG} = +0.7 \text{ V} \]

\[ V_{DD} = +3.0 \text{ V} \]

Open gate (no charge)

Lamp (no conduction)
NMOS Transistor in Conduction Mode

$V_{GG} = +0.7 \text{ V}$

$V_{DD} = +3.0 \text{ V}$

Source

Drain

Gate

$S_1$

Positive charge

Holes

$p$-type silicon substrate
Biasing Circuit for a P-Channel MOSFET

$V_{GG} = -0.7 \text{ V}$

Open gate (no charge)

Lamp (no conduction)

$V_{DD} = -3.0 \text{ V}$
PMOS Transistor in Conduction Mode

\[ V_{GG} = -0.7 \, \text{V} \]

\[ V_{DD} = -3.0 \, \text{V} \]

Negative charge

Source

Drain

I_{DS}

Lamp

p^+

Electrons

n-type silicon substrate

p^+

Gate

S_1
Schematic of a CMOS Inverter

Input

Output

$V_{DD}$

$V_{SS}$

pMOSFET

nMOSFET

$G$ $S$ $D$
Cross-section of CMOS Inverter
CMOS Manufacturing Steps

1. Twin-well Implants
2. Shallow Trench Isolation
3. Gate Structure
4. Lightly Doped Drain Implants
5. Sidewall Spacer
6. Source/Drain Implants
7. Contact Formation
8. Local Interconnect
9. Interlayer Dielectric to Via-1
10. First Metal Layer
11. Second ILD to Via-2
12. Second Metal Layer to Via-3
13. Metal-3 to Pad Etch
14. Parametric Testing
n-well Formation

- Epitaxial layer: improved quality and fewer defects
- In step 2, initial oxide (15 nm): (1) protects epi layer from contamination, (2) prevents excessive damage to ion/implantation, (3) control the depth of the dopant during implantation
- In step 5, anneal: (1) drive-in, (2) repair damage, (3) activation
Mask # 1: N-well formation
p-well Formation

- 2\textsuperscript{nd} mask, this mask is the direct opposite of the n-well implant mask
- Boron is 1/3 the mass of P, so 1/3 energy is used.
Mask # 2: P-well formation
STI Trench Etch

STI: shallow trench isolation

- Barrier oxide: a new oxide
- Nitride: (1) protect active region, (2) stop layer during CMP
- 3rd mask
- STI etching
Mask # 3: Shallow Trench Isolation formation
STI Oxide Fill

- Liner oxide to improve the interface between the silicon and trench CVD oxide
- CVD oxide deposition or spin-on-glass (SOG)
STI Formation

1. Trench oxide polish (CMP): nitride as the CMP stop layer since nitride is harder than oxide
2. Nitride strip: hot phosphoric acid
3. Anti-punch-through and Vth adjustment ion implantation
Poly Gate Structure Process

- Oxide thickness 1.5 ~ 5.0 nm is thermal grown
- Poly-Si ~ 300 nm is doped and deposited in LPCVD using SiH$_4$
- Need Antireflective coating (ARC), very critical
- The most critical etching step in dry etching
Mask # 4: Poly-Si gate formation
n⁻ LDD Implant

- LDD: lightly doped drain to reduce S/D leakage
- Large mass implant (BF₂, instead of B, As instead of P) and amorphous surface helps maintain a shallow junction
- 5ᵗʰ mask
Mask # 5: N⁻ LDD formation
p⁻ LDD Implant

- 6th mask
- In modern device, high doped drain is used to reduce series resistance. It called S/D extension
Mask # 6: P-LDD formation
Side Wall Spacer Formation

- Spacer is used to prevent higher S/D implant from penetrating too close to the channel, cover LDD.
- CVD oxide + etch back by anisotropic plasma etching
n$^+$ Source/Drain Implant

- Energy is high than LDD I/I, the junction is deep
- 7th mask
Mask # 7: N⁺ Source/Drain formation
\( p^+ \) Source/Drain Implant

- 8th mask
- Using rapid thermal **anneal** (RTA) to prevent dopant spreading and to control diffusion of dopant

Diagram:

1. Photoresist mask
2. Boron p+ S/D implant
3. Diffusion
   - Thin Films
   - Polish
   - Etch
   - Implant

Layers:
- n+ (n-well)
- p+ (p-well)
- p- Epitaxial layer
- p+ Silicon substrate
Mask # 8 : P⁺ Source/Drain formation
Contact Formation

- Titanium (Ti) is a good choice for metal contact due to low resistivity and good adhesion
- **No mask needed, called self-align**
- Using Ar to sputtering metal
- Anneal to form TiSi$_2$, tisilicide
- Chemical etching to remove unreact Ti, leaving TiSi$_2$, called selective etching
LI Oxide as a Dielectric for Inlaid LI Metal (Damascene)

- **Damascene**: a name doped of year ago from a practice that began thousands ago by artist in Damascus, Syria

LI: local interconnection
LI Oxide Dielectric Formation

- Nitride: protect active region
- Doped oxide
- Oxide polish
- 9th mask
Mask # 9: Local Interconnection formation
LI Metal Formation

• Ti/TiN is used: Ti for adhesion and TiN for diffusion barrier
• Tungsten (W) is preferred over Aluminum (Al) for LI metal due to its ability to fill holes without leaving voids
Via-1 Formation

- Interlayer dielectric (ILD): insulator between metal (800nm)
- Via: electrical pathway from one metal layer to adjacent metal layer
- 10th mask
Mask # 10: Via-1 formation
Plug-1 Formation

- Ti layer as a glue layer to hold W
- TiN layer as the diffusion barrier
- Tungsten (W) as the via
- CMP W-polish
SEM Micrographs of Polysilicon, Tungsten LI and Tungsten Plugs

Mag. 17,000 X

Micrograph courtesy of Integrated Circuit Engineering
Metal-1 Interconnect Formation

- Metal stack: Ti/Al (or Cu)/TiN is used
- Al(99%) + Cu (1%) is used to improve reliability
- 11th mask
Common gate for input

Mask # 11: Metal-1 formation

Common drain or output to next stage

P⁺ Source to Vdd

N⁺ Source to ground
SEM Micrographs of First Metal Layer over First Set of Tungsten Vias

Micrograph courtesy of Integrated Circuit Engineering
Via-2 Formation

- Gap fill: fill the gap between metal
- Oxide deposition
- Oxide polish
- 12th mask
Mask # 12: Via-2 formation
Plug-2 Formation

- Ti/TiN/W
- CMP W polish
Metal-2 Interconnect Formation

• Metal 2: Ti/Al/TiN
• ILD-3 gap filling
• ILD-3
• ILD-polish
• Via-3 etch and via deposition, Ti/TiN/W
Mask # 13: Metal-2 formation
Mask # 14: Via-3 formation
Mask # 15: Metal-3 formation
CMOS layout (mask 1 to mask 12)
Full 0.18 µm CMOS Cross Section

- Passivation layer of **nitride** is used to protect from moisture, scratched, and contamination
- **ILD-6**: oxide
SEM Micrograph of Cross-section of AMD Microprocessor

Mag. 18,250 X
Micrograph courtesy of Integrated Circuit Engineering
Wafer Electrical Test using a Micromanipulator Prober (Parametric Testing)

• After metal-1 etch, wafer is tested, and after passivation test again

• Automatically test on wafer, sort good die (X-Y position, previous marked with an red ink)

• Before package, wafer is backgrind to a thinner thickness for easier slice and heat dissipation

Photo courtesy of Advanced Micro Devices